Strength Pareto Evolutionary Algorithm for Designing and Controlling a Three-level Inverter without Balancing DC Bus Bar Voltages

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Abstract

This work deals with a Neutral Point Clamped multilevel inverter without balancing the voltage boundaries of DC bank capacitors and without dedicated EMC filters. To achieve this goal, a control over Modulated Hysteresis Current and a specific low-pass passive filter are implemented. The control strategy is associated with low and constant frequency mono carrier signal. The different components of the filter and the ones of the control are simultaneously designed by a genetic algorithm. The simulated and experimented values of voltage THD, current THD, and load power factor, underline the improvements brought by the present approach.

Keywords

Multilevel Inverter; Modulated Hysteresis Control Current MHCC; SPEA; Total Harmonic Distortion THD; EMC

Introduction

The utilization of multiple small voltage levels, especially dedicated to average and high power in industrial plants, present good power capabilities: a low total harmonic distortion of load voltage and load current, a relatively low switching losses, an effective reduction of the homopolar voltage and a satisfactory electromagnetic compatibility. On the contrary, its major disadvantages are the necessity of a larger number of power components: semiconductors and capacitors, the complexity of control circuitry and the necessity to balance the boundaries voltage of DC-bank capacitors.

The balancing of the voltage boundaries of DC bank capacitors **[**Pelletier et al (2009)**,** Mc Grath B.P. et al (2009-2009**),** Sano K. et al (2008)**]** is necessary in the purpose to achieve a high stability of the system by attenuating the low frequency ripples of the output voltage. This operation is based on the control strategy applied on the converters, using for example multicarrier PWM **[**Busquets-Monge S. et al (2009), Kouro S. et al (2008).**]**. To respect the international standards about EMC and EMI behaviors, specific filters are located in the input and in the output of these devices **[**Liu Q. et al (2007), Fujita H. (2009), Choi B. etb al (2009) , Tang Y. at al (2007), Pierquet B.J. et al (2006)**]**. Improvements are also brought about control strategies and the filters integrated into the converters **[**Lee K. et al (2008), Khajedhoddin S.A. et al (2008), Pan Z., Peng F.Z (2009), Rasoanarivo I. (2005)**]**, or the use of low switching frequency for the load current **[**Zang H. et al (2000), , Holtz J., Oikonomou N. (2008), Du Z. et al (2009)**]** .

The use of algorithm genetic is nowadays widely used in the target to optimize the operating work of a large system including static converters. Research has been carried out on the issue of sizing parameters of command and control **[**Podlubny I. (1999), Tehrani K.A. et al (2010)**]**. And thereafter, these works also take into consideration the full size of the peripheral elements of the assembly **[**Nahid-Mobarakeh B. et al (2011), Rasoanarivo I. et al (2012)**]**.

The present work deals with the application of Modulated Hysteresis Current Control (MHCC) on a Neutral Point Clamped three-level inverter, when DC voltage bus bars are not subjected to controls balancing. This article is divided into five sections. Section I develops the MHCC strategy. Section II analyses the filter. Section III applies the genetic algorithm to design simultaneously the passive elements of the filter and the control parameters. Section IV presents results of simulated functioning. Section V gives experimental tests.

Test Bench

FIG.1 presents the studied bench set: a three-phase diodes rectifier, a passive filter, a NPC three-level inverter and its load. The filter includes two coils with fluxes linked and four capacitors with midpoints connected. The DSPACE board provides the gates command of the main switches and needs consequently feedback signals: load currents i_1, i_2, i_3 and voltages v_1, v_2, v_3.

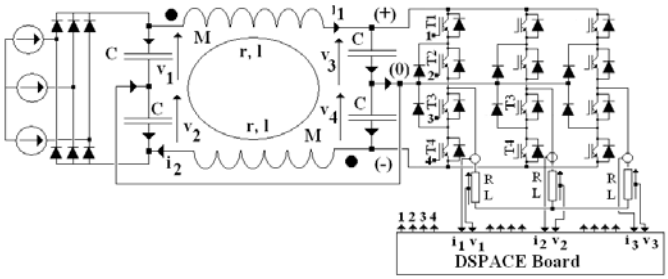

FIG.1 DIAGRAM OF THREE PHASE THREE-LEVEL NPC INVERTER SUPPLIED BY A THREE-PAHSE DIODES RECTIFIER

Control Strategy

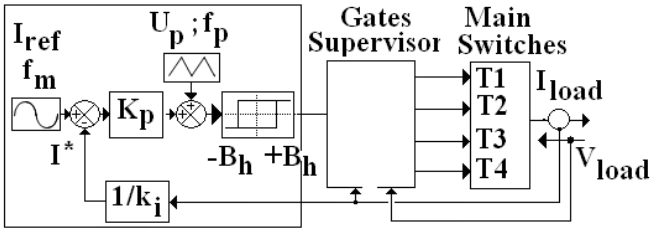

FIG.2 SYNOPTIC OF THE SUBSYSTEM BLOCK CONTROL PER PHASE

The synoptic of the control per phase is shown on FIG.2. The conventional waveforms deduced from a Modulated Hysteresis Current Control are reminded on FIG.3: the main goal is to provide one and only trigger per period of the carrier signal.

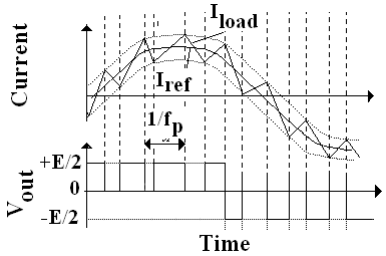

FIG.3 CONVENTIONAL WAVEFORMS IN AN INDUCTIVE LOAD FOR THE MHC CONTROL

For the current error $\varepsilon = I_{ref} - I*$, the hysteresis comparator produces the slopes instants:

$$1: if\ (K_p.\varepsilon) - u_p > B_h,\ then\ v_{out} = {}^{-E}\!/_{2}\ or\ 0; \qquad 2: if\ (K_p.\varepsilon) - u_p < -B_h,\ then\ v_{out} = {}^{E}\!/_{2}\ or\ 0 \tag{1}$$

These two conditions can also be written as:

$$\varepsilon < \frac{u_p + B_h}{K_p}\ and\ \varepsilon > \frac{-u_p + B_h}{K_p} \tag{2}$$

For an inductive load, a linear evolution of a step response (FIG.4) is practically satisfied if:

$$K_\tau = \frac{t}{\tau_e} < 0.4 \tag{3}$$

For load impedance with a minimal argument φ_{min}, in a PWM principle, the smallest value of the switching frequency to provide segment responses can be evaluated as:

$$f_{sw} = \frac{2\pi . f_m}{K_\tau . tg(\varphi_{min})},\ with\ K_\tau < 0.4 \tag{4}$$

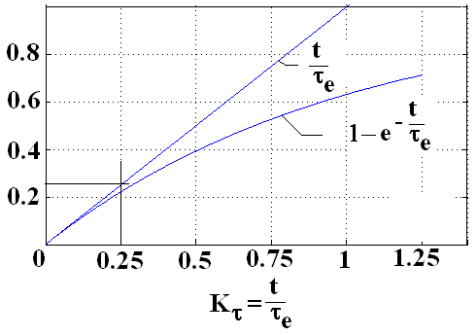

FIG.4 STEP RESPONSE EVOLUTION

In order to obtain one and only one trigger per triangular period, according to FIG.5, the error current derivative must verify the following relation:

$$\left.\frac{d\varepsilon}{dt}\right|_{min} < \frac{d\varepsilon}{dt} < \left.\frac{d\varepsilon}{dt}\right|_{max} \tag{5}$$

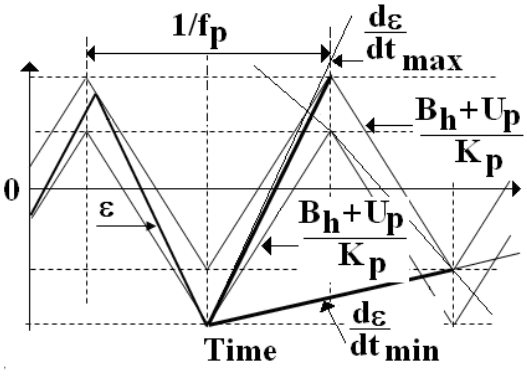

FIG.5. CURRENT ERROR EVOLUTION BETWEEN THE MODULATED HYSTERESIS BANDS

This relation is equivalent to:

$$a < \frac{B_h}{K_p} < b \tag{6}$$

Where:

$$a = \frac{1}{4 * f_p * (k_B + 1)}(2 * \pi * f_m * I_{ref\_max} + \frac{E}{2 * K_i * L});$$
$$b = \frac{1}{2 * f_p}\left| -2 * \pi * f_m * I_{ref\_max} + \frac{E}{2 * K_i * L} \right|; \quad (7)$$
$$K_B = \frac{U_{p\_max}}{B_h}$$

Equations (6) and (7) define the values of B_h / K_p in order to obtain one and only trigger per carrier period.

The present strategy needs two reference signals I_{ref} and V_{ref} which are extracted by filtering from the two load waveforms I_{load}, V_{load} as their fundamental component. Thus, the obtained waveforms are compared with an arbritrary sinus signal v_0 to determine their phase shift φ_v, φ_i . FIG.6 gives the procedure for generating these reference signals I_{ref} and V_{ref} .

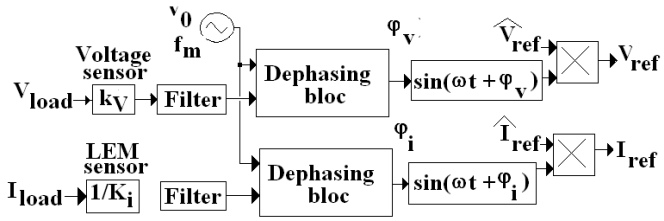

FIG.6 SCHEME TO GENERATE THE MAIN REFERENCE SIGNALS I_{ref} AND V_{ref} .

Disposing thus I_{ref} and V_{ref} , the following Boolean sentences a_i are defined:

$$a_1 = V_{ref} > 0 \ \ AND \ I_{ref} < 0;$$
$$a_2 = V_{ref} > 0 \ \ AND \ I_{ref} > 0; \quad (8)$$
$$a_3 = V_{ref} < 0 \ \ AND \ I_{ref} > 0;$$
$$a_4 = V_{ref} < 0 \ \ AND \ I_{ref} < 0;$$

The triggers gates of T_i are driven by the following equations:

$$T_1 = a_2 \ AND \ PMW$$
$$T_2 = a_2 \ OR \ (a_3 \ AND \ PMW) \quad (9)$$
$$T_3 = a_4 \ OR \ (a_1 \ AND \ PWM)$$
$$T_4 = a_4 \ AND \ PWM$$

These different operations are realized by the supervisor block presented on FIG.2

The Filter Analysis

The filter analysis takes into account the coupling modes of load. According to FIG.7, we distinguish four cases:

- Case a: three impedances connected to 0V;
- Case b: two impedances connected to (+E/2) and (-E/2), (resp. connected to (-E/2) and (+E/2)), and one to 0V;
- Case c: two impedances connected to (+E/2) (resp.(-E/2), and one to (–E/2) (resp.(+E/2));
- Case d: two impedances connected to 0V et the third to (-E/2) or (+E/2)),

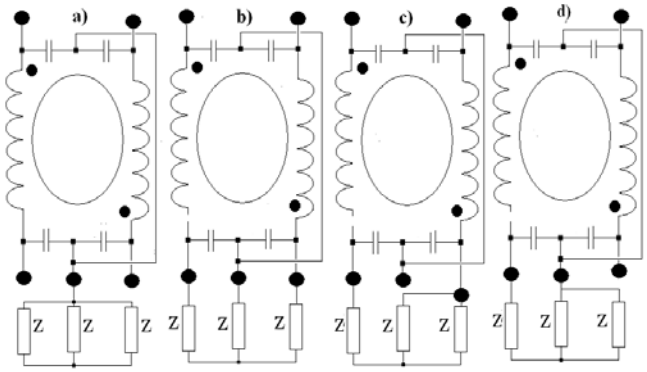

FIG.7 COUPLING MODES OF LOAD FOR THE FILTER

For Case a, by neglecting the coil resistance, the following relation defines the cut frequency:

$$\left\| \frac{(V_3 + V_4)}{E} \right\| = \frac{1}{1 - \omega^2 . C . (L + M)} \quad (10)$$

Thus::

$$\omega_o = \frac{1}{\sqrt{C . (L + M)}} \quad (11)$$

And for the other cases, for appropriated values of the coils and the capacitor parameters, we must have:

$$lim_{\omega \to 0} \left\| \frac{V_3}{E} \right\| = lim_{\omega \to 0} \left\| \frac{V_4}{E} \right\| = \frac{1}{2} \quad (12)$$

The SPEA Analysis

In the optimization problems of control systems normally simultaneous optimization, different and often conflicting objectives are needed. In this case there is a set of optimal solutions instead of a single one. The set, representing non-dominated solutions, is known as Pareto Optimal Set (POS), and the set of the corresponding values of the objective functions is called Pareto Optimal Front (POF). Pareto-based evolutionary algorithms:

1- Produce a random parent population *P* and form the empty external non-dominated set *P'*.
2- Paste non-dominated members of P into P'
3- Eliminate all solutions within P' which are covered by any other members of P'.

4- If the number of externally stored non-dominated solutions exceeds a given maximum N', use clustering to prune P'.

5- Assigns fitness to all individuals in P and P'.

6- Select individuals from P and P' using binary tournament selection with replacement until the mating pool is filled.

7- Apply genetic operators (crossover and mutation) as usual.

8- If the maximum number of generations is reached, then stop, else go to step 2.

In this work, the SPEA method allows the dimensioning of different elements of the bench set. These elements define the optimization variable $[X]$ which are for the filter components $: L, M, C$, and for the MHCC parameters: U_p, f_p, K_p, K_I, B_h.

The objective functions $[F]$ are defined as follows:

a. The MHCC is effective: perfect control of the current and a low and constant switching frequency;

b. The DC bus bar voltages are symmetrical, and are free from high ripples;

c. The total harmonic distortion of load voltage THD_V is satisfactory and the current THD_I is relatively small.

To make quick convergence of calculations, the optimization variables must be defined within intervals enclosed minimum and maximum values. For the filter, a small size of the inductor imposes L about a few ''mH''. And with a low cut frequency (Eq.11), we obtain C. For the control, we apply the relations of Eq.6 and Eq.7 to define its parameters, for a DC bus bar voltage and load given. In addition, the carrier signal frequency must be defined by Eq.4. The other data are: supply voltage $230V$, frequency of modulating wave: $50Hz$, load $Z = 6e^{j15°}\Omega$, reference current $\bar{I}_{ref} = 40A$. For the optimization calculations, the number of the POF solutions is equal to 5, and the one of generation 3. TABLE 1 gives thus the values of the POF solutions for third and last generation.

As viewed on TABLE 1, the solutions POF3 present the most interesting objective functions. The value of the inductor is smaller than $2mH$. The switching frequency is $1852Hz$ smaller than the value calculated from Eq.4 which is equal to $2300Hz$. The two voltages V_3 and V_4 are perfectly symmetrical (FIG.8) and their ripples are around $10V$. The load THD_I is very small and the load THD_V about 45%. FIG.8 shows the waveforms associated with POF3 solutions. On this figure, the load current is sinusoidal. The voltage V_{10} between the phase *1* and the midpoint of the bank capacitor is very clean and presents constant frequency commutations.

TABLE 1 PARETO OPTIMAL FRONT SETS AFTER THIRD GENERATION

		POF1	POF2	POF3	POF4	POF5
Opt. variables	L(mH)	2,97	2,22	1,50	1,98	3,17
	M(mH)	2,72	2,1	1,34	1,78	2,85
	C(µF)	3294	4068	3834	3964	3347
	Up(V)	0,15	0,17	0,20	0,25	0,14
	K I	26,62	27,89	31,48	27,25	30,91
	Kp	14,25	15,14	6,13	11,38	14,70
	Bh	0,035	0,038	0,043	0,032	0,034
	fsw(Hz)	2498	2492	1852	1425	2801
Obj. functions	Iref peak (A)	42,46	41,66	38,63	42,41	39,29
	THDi(%)	4,52	3,21	2,61	3,22	2,66
	THDv(%)	41,67	40,12	44,90	38,98	44,94
	V3(V)	272	274,8	276,9	274,3	274,2
	V4(V)	276	280,6	276,7	279,6	276,1
	ΔV3 (V)	60	15	12	50	15
	ΔV4 (V)	55	20	14	45	10

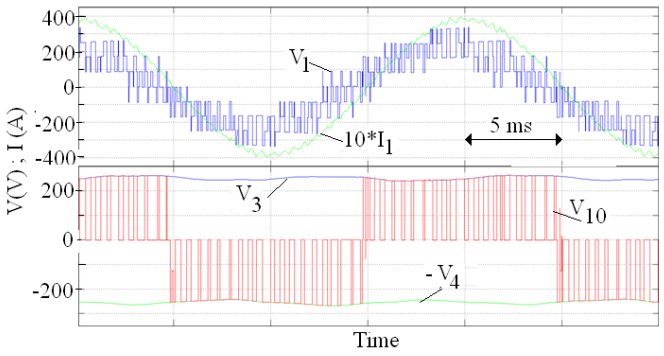

FIG.8 WAVEFORMS CORRESPONDING TO THE SOLUTION POF3

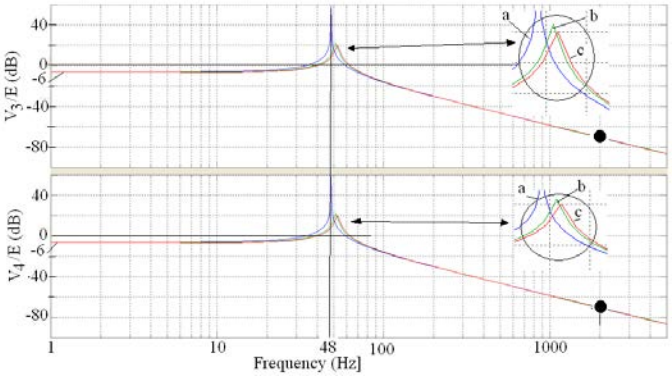

FIG.9 BODE DIAGRAM OF THE FILTER WITH THE SOLUTIONS POF3

FIG.9 shows the Bode diagram of V_3 / E and V_4 / E, associated with the configurations cases a, b and c shown on FIG.7, The relation given by Eq.12 ($-6dB$ at $0Hz$), and the value of the cut frequency ($48Hz$) defined by Eq.11 are well verified. In addition, it notes an attenuation of $-70dB$ at $2000Hz$.

Simulation

For current and voltage with harmonic components:

$$i(t)=\sum_{k=1}^{\infty} I_{2k+1}\sin((2k+1).\omega.t+\alpha_{2k+1}) \qquad (13)$$
$$v(t)=\sum_{k=1}^{\infty} V_{2k+1}\sin((2k+1).\omega.t+\beta_{2k+1})$$

the global form factor is defined by:

$$\lambda_G=\frac{1}{\sqrt{1+THD_I^2}.\sqrt{1+THD_V^2}} \qquad (14)$$

The global form factor λ_G represents the influence of the harmonic values contained in these waveforms in relation to the power capabilities of the multilevel inverter.

The simulation is carried out with the solutions POF3 given on TABLE 1. The main goal is to extend the operating values in order to delimit the areas of validation of the objective functions defined in paragraph describing the SPEA analysis. This concerns the load $Z=|Z|e^{j\varphi^\circ}$, the reference current $\hat{\bar{I}}_{ref}$, and the filter capacitor C. For each simulation, four families of curves are plotted:

1. Curves of DC positive bus bar voltage V_3, and the ones of negative bus bar voltage $-V_4$;
2. Curves of the ripples of DC bus bar positive voltage ΔV_3, and the ones of DC bus bar negative voltage ΔV_4;
3. Curves of the line current $\hat{\bar{I}}_1$ of the phase 1;
4. Curves of the global form factor λ_G;

Note that in order to match with the experimental tests, the supply voltage is $130V$.

Influence of the load

The data are: $\hat{\bar{I}}_{ref}=20A$; $|Z|=2{,}5;5;7{,}5;10\Omega$; $Arg(Z)=15;30;45;60;75°$. On FIG.10, curves '1' show that V_3 and $-V_4$ are perfectly symmetrical, and their ripples don't exceed $16V$ (curves '2') which are stronger in low argument than those in high argument.

On curves '3', line current $\hat{\bar{I}}_1$ deviates slightly from the reference value. Expect for $|Z|=2{,}5\Omega$, the global form factor λ_G is around 0.9 and appears as independent of the load parameters. So, we can deduce that the two DC bus bar voltages are symmetrical. Their ripples have no significant influence on the global form factor λ_G which remains interesting and practically constant.

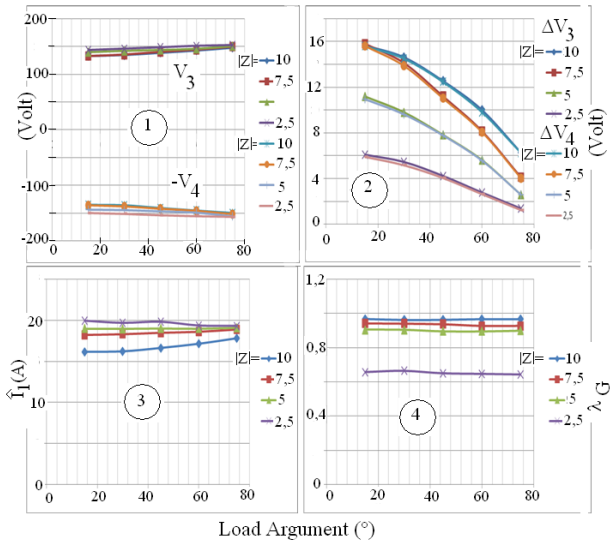

FIG.10 CURVES VERSUS THE LOAD PARAMETERS

Influence of the Reference Current

The data are: $\hat{\bar{I}}_{ref}=10;20;30;40A$; $|Z|=3;4;5\Omega$; $Arg(Z)=30°$. On FIG.11, curves '1' show also that V_3 and $-V_4$ are symmetrical, and present linear drop voltage. Theirs ripples are identical and increase with the current (curves '2'). Curves '3' show that the line current $\hat{\bar{I}}_1$ is proportional with the reference current, but deviates strongly at high value of Z and line current. Expect for $\hat{\bar{I}}_{ref}=10A$, the global form factor λ_G is practically constant around 0.92, and appears independent of the ripples of the two DC bus bar voltages (curves '4').

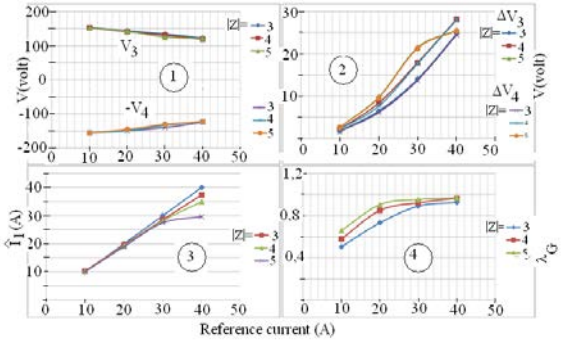

FIG.11 CURVES VERSUS THE REFERENCE CURRENT

Influence of the Capacitor C

The data are: $\hat{I}_{ref} = 10;20;30;40A$; $Z = 5\Omega e^{j30°}$; $C = 3300;4700;6800\mu F$. The curves of V_3 and $-V_4$ shown on FIG.11 are practically identical with those given on FIG.10. However, the voltage drops are smaller for great values of the capacitor. The curves of ΔV_3 , ΔV_4 , $\hat{I}_1$, and λ_G present also the same evolutions. In addition, it is relevant to note that the global form factor λ_G is practically independent of the capacitor, and remains greater than $O.92$ from $\hat{I}_1 < 20A$.

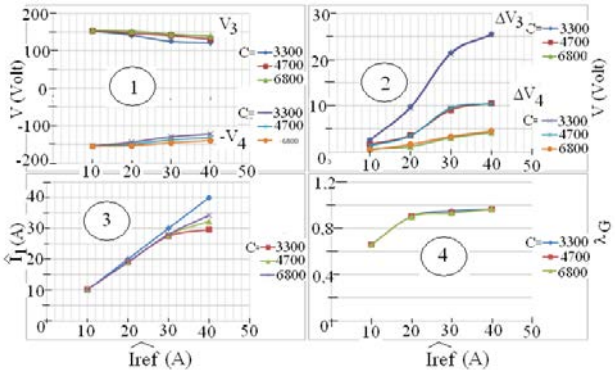

FIG.11 CURVES VERSUS THE CAPACTOR OF THE FILTER AND THE REFERNCE CURRENT $\hat{I}_1$

Experimental Tests

FIG.12 presents the photography of the test bench with the DSPACE 1104 device.

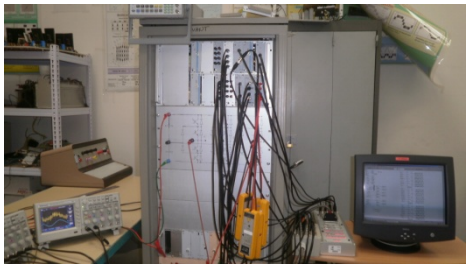

FIG.12 TEST BENCHWITH DSPACE 1104 BOARD

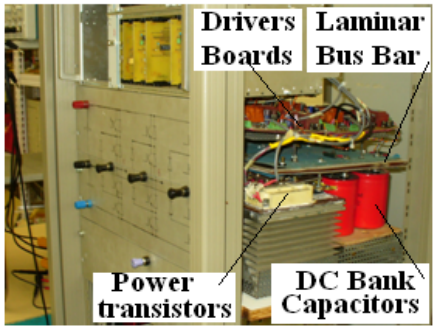

FIG.13 PHOTOGRAPHY OF THE CONVERTER AND ITS DIFFERENT ELEMENTS

On FIG.13, the NPC structure is plotted in the face panel. Behind this panel, the DC bank capacitors have no balancing circuits. The laminar bus bar is used to connect the power transistors and the DC bank capacitors [Lounis Z., Rasoanarivo I., Davat B.], with $C = 6600\mu F$. The carrier frequency is $1800Hz$ and the reference current is $20A$.

FIG.14 and 15 present experimental gates triggers per arm of the inverter. On FIG.14, triggers $T1$ (resp. triggers $T4$) are well generated during $V_1 * I_1 > 0$ (resp. $V_1 * I_1 < 0$).

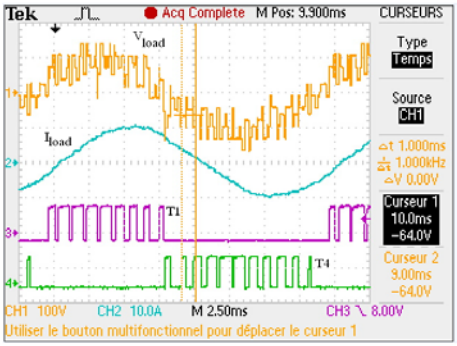

FIG.14. TRIGGERS T1 AND T4 FACING THE WAVEFORMS OF V_1 AND I_1

On FIG.15, triggers $T2$ (resp. triggers $T3$) are produced during the positive alternation (resp. the negative alternation) of the line current. These waveforms validate perfectly the Boolean equations described in Eq.8 and Eq.9. It is interesting to highlight that these triggers commutate cleanly with constant period.

From FIG.16 to FIG.19 are presented experimental waveforms of load phase voltage and line current for different load impedances. On these figures, the voltage patterns present small steps perfectly flat and are cleanly commutated. In addition, line currents are sinusoidal, thus validating the results shown of FIG.8: the current control is efficient and the current shapes are independent of the load parameters.

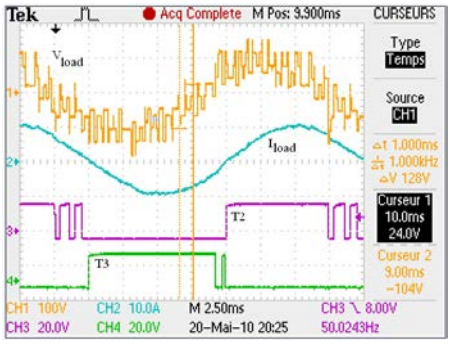

FIG.15 TRIGGERS T2 AND T3 FACING THE WAVEFORMS OF V_1 AND I_1

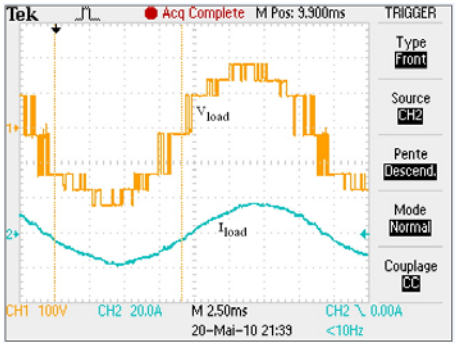

FIG.16 WAVEFORMS OF V_1 AND I_1 WITH $Z_1 = 9e^{j16.07°}$

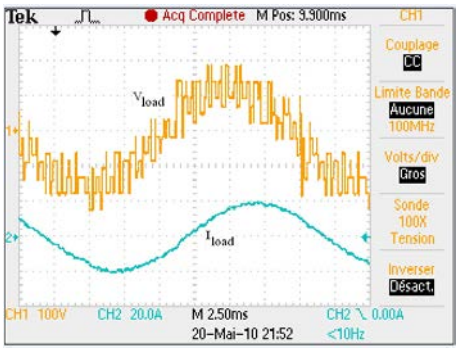

FIG.17 WAVEFORMS OF V_1 AND I_1 WITH $Z_2 = 7e^{j37.66°}$

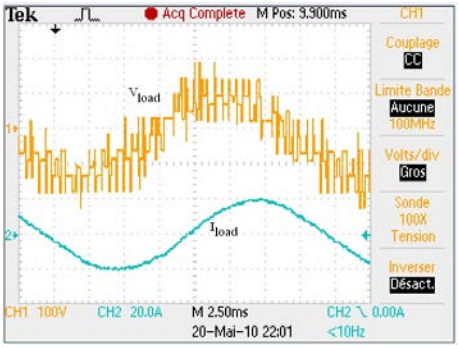

FIG.18 WAVEFORMS OF V_1 AND I_1 WITH $Z_3 = 5.8e^{j48.47°}$

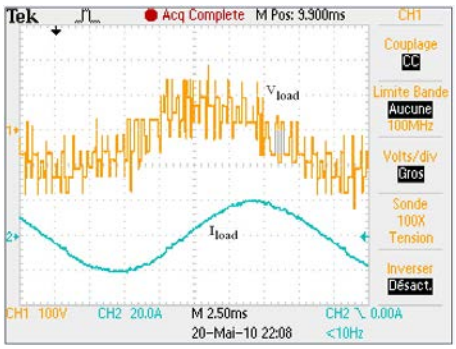

FIG.19 WAVEFORMS OF V_1 AND I_1 WITH $Z_4 = 5e^{j63.56°}$

The total harmonic distortion of current THD_I given on FIG.20 presents satisfactory values, below 5%. On contrary, the total harmonic distortion of phase voltage THD_V is enough bad especially for high value of load argument. Finally, FIG.21 presents the global form factor versus the load parameters. Its value is more than $O.85$, and underlines that the good capabilities of multilevel inverter are well kept. This quantity is better for low argument load, thus signifying a transfer of active power as great as possible.

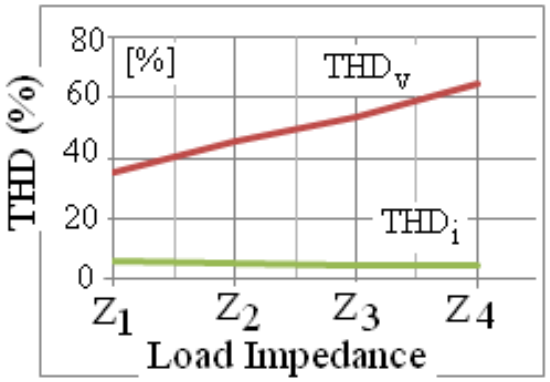

FIG.20 TOTAL HARMONIC DISTORTION OF OUTPUT PHASE VOLTAGE THDv AND LINE CURRENTS THDi VERSUS LOAD

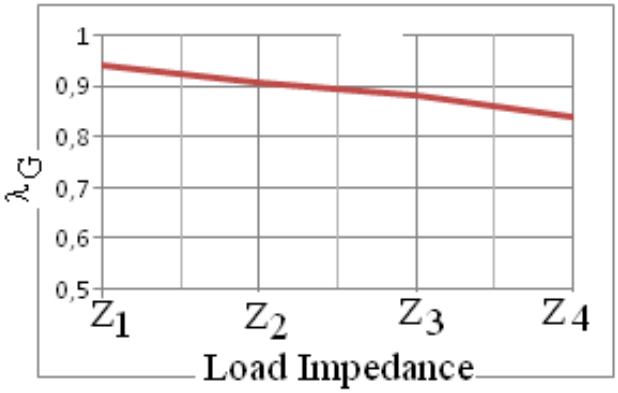

FIG.21 GLOBAL FORM FACTOR λ_G VERSUS LOAD

Conclusions

The results given by simulation highlight clearly the simultaneous actions of the proposed passive filter and the control of the inverter.

The SPEA optimization gives POF solutions acceptable to have a good working of the bench, defined from an operating point associated with the maximum power of load. And the analysis is carried out for another functioning point inferior than this maximum point.

In spite of the low value of the inductor of the filter and tne one of the swicthing frequency in the range of the capacitor values, , the low value of the switching frequency, the DC bus bar voltages are perfectly symmetrical. On contrary, the drop voltage and its ripples depend on the filter capacitor C.

In addition, the approach developed in this work doesn't degrade the capabilities of the NPC inverter even if the DC bank capacitors boundaries are not controlled. The global form factor is practically independent of the DC ripples voltage.The waveforms obtained from simulation and from experimentation are perfectly in good correspondence. In spite of a mono carrier signal and low switching frequency, the control strategy effectively delivers sinusoidal line current. The different levels of the output voltage are flat and are independent of the load argument.

The waveforms of line currents and its *THD* show a better behavior about differential conducted mode. A voltage *THD* around *50%* is significant of a poor harmonic content for the phase voltage, meaning a good behavior of common conducted mode. In these cases, EMI and EMC filters are not obligatory necessary.

Finally, the global form factor, which is proportional to power factor appears effectively excellent. The balancing of the banc capacitors is not necessarily useful, when the MHCC strategy is applied: the parameters of energy conversion of the three phase three-level NPC inverters are satisfying, and thanks to the low switching frequency, the efficiency of the device is also improved.

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